Workshop Proposal for HUIC 2011

Ultra-Low Power Asynchronous Digital Circuits

Topic/Area: Low Power VLSI Design

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Abstract

The development of synchronous circuits currently dominates the semiconductor industry. However, as clock rates have significantly increased while feature size has decreased, clock-induced problems such as clock distribution, clock tree power, and difficulties in reaching timing closure, have become major challenges of synchronous circuits. Hence, the 2009 International Technology Roadmap for Semiconductors (ITRS) predicts that asynchronous (clockless) circuits will occupy 17% of the world's total IC area in 2010, 30% in 2016, and 49% in 2024, which is a substantial portion of this multi-billion dollar industry. To meet this growing industry need, chip designers should familiarize themselves with asynchronous design to make themselves more marketable and more prepared for the challenges faced by the digital design community for years to come.

ITRS states that "power consumption is now one of the major constraints in chip design, and ITRS has identified it as one of the top three overall challenges for the last 5 years. Leakage power consumption, including its variability, has been identified as a clear long term threat and a focus topic for design technology in the next 15 years." With the current trend of semiconductor devices scaling into the deep submicron region, design challenges that were previously minor issues have now become increasingly important. Where in the past, dynamic, switching power has been the predominant factor in CMOS digital circuit power dissipation, recently, with the dramatic decrease of supply and threshold voltages, a significant growth in leakage power demands new design methodologies for digital integrated circuits (ICs). The main component of leakage power is sub-threshold leakage, caused by current flowing through a transistor even when it is supposedly turned off. Sub-threshold leakage increases exponentially with decreasing transistor feature size.

Among the many techniques proposed to control or minimize leakage power in deep submicron technology, Multi-Threshold CMOS (MTCMOS), which reduces leakage power by disconnecting the power supply from the circuit during idle (or sleep) mode while maintaining high performance in active mode, is very promising. MTCMOS incorporates transistors with two or more different threshold voltages (V_t) in a circuit. Low-V_t transistors offer fast speed but have high leakage, whereas high-V_t transistors have reduced speed but far less leakage current. MTCMOS combines these two types of transistors by utilizing low-V_t transistors for circuit switching to preserve performance and high-V_t transistors to gate the circuit power supply to significantly decrease sub-threshold leakage. Quasi-delay-insensitive (QDI) NULL Convention Logic (NCL) circuits designed using CMOS exhibit an inherent idle behavior since they only switch when useful work is being performed; however, there is still significant leakage power during idle mode.

This workshop will provide an introduction to asynchronous logic, NULL Convention Logic (NCL), and Multi-Threshold CMOS (MTCMOS), and then detail how the MTCMOS technique is combined with NCL to yield a fast ultra-low power asynchronous circuit design methodology, called Multi-Threshold NULL Convention Logic (MTNCL), which vastly outperforms traditional NCL in all aspects (i.e., area, speed, energy, and leakage power), and significantly outperforms the MTCMOS synchronous architecture in terms of area, energy, and leakage power, although the MTCMOS synchronous design can operate faster.

Participants need not have any prior knowledge of asynchronous circuit design, but should be familiar with basic logic design concepts, such as Boolean algebra, Karnaugh maps, and transistor-level digital design. At the end of this workshop, participants will be familiar with the advantages of asynchronous circuits, the power challenges facing the semiconductor industry, and the challenges to asynchronous design being integrated into the mainstream semiconductor design industry, and will know how to design ultra-low power MTNCL circuits and systems.

Key Words: VLSI, Asynchronous Logic, NULL Convention Logic (NCL), Multi-Threshold CMOS (MTCMOS), Multi-Threshold NULL Convention Logic (MTNCL), Low Power Design

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† The author gratefully acknowledges the support from the National Science Foundation under CCLI grants DUE-0536343, DUE-0717572, and DUE-0717767.